

Claims

- 1 1. An electronic display comprising:
 2 an encapsulated display medium comprising a plurality of pixels;
 3 a transistor having a data electrode, a gate electrode and a pixel electrode and
 4 comprising a layer of insulating material situated between a first layer of conductive
 5 material that forms the gate electrode and a second layer of conductive material that
 6 forms the data and pixel electrodes, the transistor applying an addressing voltage to
 8 a storage capacitor comprising a layer of insulating material situated between a first
 9 layer of conductive material and a second layer of conductive material, said storage
 10 capacitor in electrical communication with the pixel addressed by the transistor for
 11 reducing a rate of voltage decay across the pixel.
- 1 2. The display of claim 1 wherein each of said pixels comprises an electrophoretic
 2 display medium comprising at least one capsule containing particles disposed in a
 3 fluid.
- 1 3. The display of claim 1 wherein one of said layers of material comprising said
 2 transistor and a respective layer of material comprising said storage capacitor
 3 comprise a continuous layer of material.
- 1 4. The display of claim 1 wherein said transistor and said storage capacitor each further
 2 comprise a layer of semiconducting material situated between said respective first
 3 layers of conductive material and said respective second layers of conductive
 4 material.
- 1 5. The display of claim 4 wherein one of said layers of material comprising said
 2 transistor and a respective layer of material comprising said storage capacitor
 3 comprise a continuous layer of material.
- 1 6. The display of claim 4 wherein said transistor and said storage capacitor comprise a
 2 plurality of continuous layers of material.

Sub Q3
7. The display of claim 1 wherein the storage capacitor is in electrical communication with a second gate line different from a first gate line in electrical communication with the transistor gate electrode for addressing the pixel.

1 8. The display of claim 1 wherein the storage capacitor is in electrical communication
2 with a conductor.

1 9. The display of claim 1 wherein the storage capacitor comprises a storage capacitor
2 pixel electrode, an insulator disposed adjacent the pixel electrode and a storage
3 capacitor gate electrode disposed adjacent the insulator.

Sub Q4
1 10. The display of claim 9 wherein the insulator is patterned.

1 11. The display of claim 9 wherein the insulator is unpatterned.

1 12. The display of claim 9 wherein the insulator forms a part of the storage capacitor and
2 the transistor.

1 13. The display of claim 1 wherein the storage capacitor comprises a storage capacitor
2 pixel electrode, a semiconductor layer disposed adjacent the storage capacitor pixel
3 electrode, an insulator layer disposed adjacent the semiconductor, and a storage
4 capacitor gate electrode disposed adjacent the insulator.

1 14. The display of claim 1 wherein the storage capacitor comprises a storage capacitor
2 pixel electrode, an insulator disposed adjacent the storage capacitor pixel electrode
3 and a conductor disposed adjacent the insulator.

1 15. The display of claim 1 wherein a capacitance of the storage capacitor is greater than a
2 capacitance of the pixel.

Sub Q5
1 16. The display of claim 1 wherein a voltage decay time across the pixel is based on the
2 product of R_p and $(C_p + C_s)$ where R_p is a resistance of the pixel, C_p is a capacitance
3 of the pixel, and C_s is a capacitance of the storage capacitor.

1 17. The display of claim 1 wherein said transistor and said storage capacitor comprise a
2 plurality of continuous layers of material.

Sub Q6
1 18. An electronic display comprising:

an encapsulated electrophoretic display medium comprising a plurality of pixels; and
a storage capacitor comprising a layer of insulating material situated between a first
layer of conductive material and a second layer of conductive material, said storage
capacitor in electrical communication with one of said plurality of pixels for
reducing a rate of voltage decay across the pixel.

19. A method of addressing an electronic display having a display medium comprising a
plurality of pixels and a plurality of storage capacitors, at least one of said plurality of
storage capacitors in electrical communication with a corresponding one of said
plurality of pixels, the method comprising:

applying an electric pulse to the pixel and storage capacitor to charge the pixel and
storage capacitor to an addressing voltage, the duration of the electric pulse being
insufficient in length to fully address the pixel directly, so that the pixel is addressed
and presents an intended appearance after the electric pulse ends.

20. The method of claim 19 wherein a plurality of electric pulses are successively applied
to a plurality of pixels and storage capacitors, each pulse charging the respective pixel
and storage capacitor to an addressing voltage of the corresponding pixel, an
individual duration of an electric pulse being insufficient in length to fully address a
pixel directly, so that the pixels are addressed and present an intended image after the
electric pulses end